OpenMP Implementations
For FUJITSU Supercomputer
PRIMEHPC FX100

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OpenMP®
and VISIMPACT™
implemented in PRIMEHPC FX100

- Key technologies for the Exascale era
- Enabling Efficient Hybrid Parallelization
- Creating synergy with Explicit Vector Programming
Thread Affinity Control of OpenMP 4.0

To fit the ccNUMA architecture, first, spread two threads among CMGs. Second, place 15 threads close to the parent thread.

```
export OMP_PLACES="{0:16},{16:16}"

!$omp parallel proc_bind(spread)
!$omp parallel proc_bind(close)
!$omp end parallel
!$omp end parallel
```
Explicit Vector Programming Using SIMD Constructs of OpenMP 4.0

HPC-ACE2: ISA enhancements

- Wider SIMD enhancements from K computer / FX10
  - 256-bit wide SIMD (64-bit x 4 / 32-bit x 8)
  - More integer operations
  - Stride load/store
  - Indirect load/store
  - Compress
  - Round
  - Permutation


SIMD constructs of OpenMP 4.0 are useful to make use of the 256-bit wide SIMD instructions.

```c
#pragma omp declare simd
float fmax(float a, float b) {
    return (a < b ? b : a);
}

void vfmax(float *r, float *p, float *q) {
    #pragma omp parallel for simd
    for (t = 0; t < SIZE; t++) {
        r[t] = fmax(p[t], q[t]);
    }
}
```
Version 3.0 in Japanese now available on the web.

- **Version 3.0, Japanese** (updated January 13, 2009) (PDF) Translation by engineers from Fujitsu, and reviewed by Dr. Satoh of the University of Tsukuba, and volunteers at NEC.

Version 4.0 in Japanese is expected by many Japanese users.

- Targeting to publish by SC15
- Calling for Volunteers!
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